CLAIMS

1. A digital signal processor comprising:

a core processor;

a level one memory for operation with the core processor;

a store buffer configured to hold write information, generated by the core processor, for the level one memory and for a level two memory, the store buffer having a store buffer capacity;

a write buffer configured to hold write information, received from the store buffer, for the level two memory, the write buffer having a normal capacity and an excess capacity; and

a memory controller configured to enable the excess capacity of the write buffer when a high priority task is being serviced and to inhibit write access to the excess capacity of the write buffer when a high priority task is not being serviced.

2. A digital signal processor as defined in claim 1, wherein the high priority task is an interrupt handler.

3. A digital signal processor as defined in claim 1, wherein the excess capacity of the write buffer is equal to or greater than the effective store buffer capacity.

4. A digital signal processor as defined in claim 1, wherein the memory controller is configured to transfer the contents of the store buffer to the write buffer when the high priority task is invoked.

5. A digital signal processor as defined in claim 4, wherein the memory controller is configured to stall the core processor when the high priority task is completed and to write the contents of the write buffer to memory until the write information held in the write buffer no longer uses the excess capacity.

6. A digital signal processor as defined in claim 5, wherein the memory controller is configured to increase the priority of write operations to the level two memory when the core processor is stalled following completion of a high priority task.

7. A digital signal processor as defined in claim 1, further comprising a second write buffer configured to hold write information for a level three memory and to receive the write information from the first-mentioned write buffer.

8. A digital signal processor comprising:

a core processor;

a relatively fast memory for operation with the core processor;

a store buffer configured to hold write information, generated by the core processor, for the relatively fast memory and for a relatively slow memory, the store buffer having a store buffer capacity;

a write buffer configured to hold write information, received from the store buffer, for the relatively slow memory, the write buffer having a normal capacity and an excess capacity; and

a memory controller configured to enable the excess capacity of the write buffer and to transfer contents of the store buffer to the write buffer

when a high priority task is invoked and to inhibit write access to the excess capacity of the write buffer when a high priority task is not being serviced.

9. A digital signal processor as defined in claim 8, wherein the high priority task is an interrupt handler.

10. A digital signal processor as defined in claim 8, wherein the excess capacity of the write buffer is equal to or greater than the effective store buffer capacity.

11. A digital signal processor as defined in claim 8, wherein the memory controller is configured to stall the core processor when the high priority task is completed and to write the contents of the write buffer to memory until the write information held in the write buffer no longer uses the excess capacity.

12. A digital signal processor as defined in claim 11, wherein the memory controller is configured to increase the priority of write operations to the relatively slow memory when the core processor is stalled following completion of a high priority task.

13. A method for operating a digital signal processor comprising:

providing a digital signal processor including a core processor, a level one memory for operation with the core processor, and a store buffer configured to hold write information for the level one memory and for a level two memory;

providing a write buffer, configured to hold write information, received from the store buffer, for the level two memory, having a normal capacity and an excess capacity;

enabling the excess capacity of the write buffer and transferring the contents of the store buffer to the write buffer when a high priority task is invoked; and

inhibiting write access to the excess capacity of the write buffer when a high priority task is not being serviced.

14. A digital signal processor comprising:

a core processor;

a level one memory for operation with the core processor;

a first fill buffer configured to hold read data in a fill operation;

a second fill buffer configured to hold read data in a fill operation; and

a memory controller configured to steer read data to the first fill buffer or the second fill buffer based on priority of the fill operation.

15. A digital signal processor as defined in claim 14, wherein the memory controller is configured to steer read data to the first fill buffer or the second fill buffer according to an address of the fill operation.

16. A digital signal processor as defined in claim 15, wherein an address criteria for steering read data to the first fill buffer or the second fill buffer in a fill operation is programmable.

17. A digital signal processor as defined in claim 16, wherein the address criteria for steering read data comprises a descriptor associated with each memory page.

18. A digital signal processor as defined in claim 14, wherein the level one memory comprises a cache memory and the fill operation comprises a cache line fill operation.

19. A digital signal processor as defined in claim 14, wherein the level one memory comprises a random access memory and wherein the fill operation comprises a word replacement operation.

20. A digital signal processor as defined in claim 14, wherein the memory controller is configured to steer low priority read data to the first fill buffer and to steer high priority read data to the second fill buffer.

21. A digital signal processor as defined in claim 14, wherein the memory controller is configured to steer low priority read data to the first fill buffer and to steer high priority read data to an available one of the fill buffers.

22. A method for operating a digital signal processor comprising:

providing a digital signal processor including a core processor and a level one memory for operation with the core processor;

providing first and second fill buffers for holding read data in a fill operation; and

steering read data to the first fill buffer or the second fill buffer based on priority of the fill operation.

23. A method as defined in claim 22, wherein read data is steered to the first fill buffer or the second fill buffer according to an address of the fill operation.

24. A method a defined in claim 23, wherein an address criteria for steering read data to the first fill buffer or the second fill buffer is programmable.

25. A method as defined in claim 24, wherein the address criteria for steering read data comprises a descriptor associated with each memory page.

26. A method as defined in claim 22, wherein the level one memory comprises a cache memory and wherein the fill operation comprises a cache line fill operation.

27. A method as defined in claim 22, wherein the level one memory comprises a random access memory and wherein the fill operation comprises a word replacement operation.

28. A method as defined in claim 22, wherein steering read data comprises steering low priority read data to the first fill buffer and steering high priority read data to the second fill buffer.

29. A method as defined in claim 22, wherein steering read data comprises steering low priority read data to the first fill buffer and steering high priority read data to an available one of the fill buffers.

30. A digital signal processor comprising:

a core processor;

a level one memory for operation with the core processor;

a store buffer configured to hold write information, generated by the core processor;

a first write buffer configured to hold write information, received from the store buffer, for a level two memory;

a second write buffer configured to hold write information, received from the store buffer, for a level three memory; and

a memory controller configured to steer write information to the first write buffer or the second write buffer based on an address of a write operation.

31. A digital signal processor as defined in claim 30, wherein at least one of the write buffers has a normal capacity and an excess capacity and wherein the memory controller is configured to enable the excess capacity when a high priority task is being serviced and to inhibit write access to the excess capacity when a high priority task is not being serviced.

32. A digital signal processor as defined in claim 31, wherein the high priority task comprises an interrupt handler.

33. A digital signal processor as defined in claim 31, wherein the excess capacity is equal to or greater than an effective capacity of the store buffer.

34. A digital signal processor comprising:

a core processor;

a level one memory for operation with the core processor;

a first buffer configured to hold write information, received from the core processor, for the level one memory;

a second buffer configured to hold write information, received from the core processor, for a level two memory; and

a memory controller configured to steer the write information to the first buffer or the second buffer based on an address of a write operation.

35. A digital signal processor as defined in claim 34, wherein the first and second buffers each comprise a store buffer and a write buffer.

36. A digital signal processor as defined in claim 34, further comprising a third buffer configured to hold write information, received from the core processor, for a level three memory.